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Inkjet-Printing-Based Soft-Etching Technique for High-Speed Polymer Ambipolar Integrated Circuits

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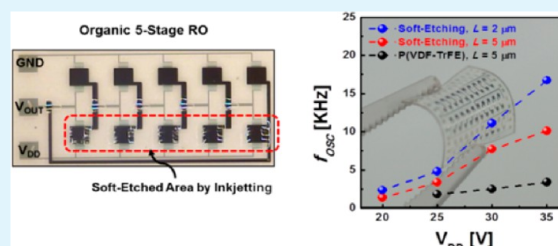
Supporting Information

ABSTRACT: Here, we report the so-called soft-etching process based on an inkjet-printing technique for realizing high-performance printed and flexible organic electronic circuits with conjugated polymer semiconductors. The soft-etching process consists of selective etching of the gate made of a dielectric polymer and deposition of another gate dielectric layer. The method enables the use of a more desirable polymer dielectric layer for the p-channel and n-channel organic field-effect transistors (OFETs) in complementary integrated circuits. We fabricated high-performance ambipolar complementary inverters and ring oscillators (ROs) using poly([*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)) (P(NDI2OD-T2)) as the active layer as well as poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) and polystyrene ((PS)/P(VDF-TrFE)) as dielectric materials for the p-channel (pull-up transistor) and n-channel (pull-down transistor) OFETs, respectively. The PS dielectric polymer was selectively etched by inkjetting of *n*-butyl acetate as an orthogonal solvent for P(NDI2OD-T2). Employing this methodology, the five-stage ambipolar ROs with P(NDI2OD-T2) exhibited an oscillation frequency of ∼16.7 kHz, which was much higher than that of non-soft-etched ROs with a single dielectric layer (P(VDF-TrFE); ∼3 kHz).



KEYWORDS: *organic field-effect transistors, inkjet printing, ambipolar semiconductor, ambipolar integrated circuits, patterning process, gate dielectric*

INTRODUCTION

Organic field-effect transistors (OFETs) based on ambipolar semiconductors have attracted great interest from both academic and industrial fields over the past decade.[1−3] The OFETs' ability to accumulate and transport carriers of both holes and electrons using a single molecule in electronic and optoelectronic devices paves the way to understanding π-conjugated materials and device physics as well as realizing a variety of functional applications such as organic light-emitting transistors,[4,5] photoactive sensors,[6] and ambipolar complementary integrated circuits (ICs).[7−14] Several research groups have reported the development of a number of ambipolar organic semiconductors and their use in electronic circuits.[7−14] Organic ambipolar complementary circuits still face a few challenges, including the unbalanced field-effect mobilities (μ_{FET}) and threshold voltages (V_{Th}) for holes and electrons as well as the difficulty in achieving efficient hole and electron injection from Au, resulting in asymmetric voltage-transfer characteristics (VTCs) of an inverter. More importantly, some amount of standby power is dissipated in such ambipolar inverters because neither pull-up nor pull-down transistors are fully turned off when the counterpart transistor is switched on.

Recently, several approaches have been reported to overcome the above challenges by optimizing the molecular design for well-balanced values of hole and electron μ_{FET}, introducing an interlayer for efficient charge injection, and engineering the gate dielectric interface.[11−14] For balanced hole and electron transporting and low-voltage operation in ambipolar ICs, our group reported the investigation on a high-permittivity (k) polymer blend for the dielectric layer composed of a fluorinated high-k dielectric, poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)), and low-k conventional dielectrics, polystyrene (PS) and poly(methyl methacrylate) (PMMA).[13] The large dipole moment of the asymmetrically attached −C−F side chain in P(VDF-TrFE) enabled enhanced accumulation of holes at the semiconductor−dielectric interface by bending

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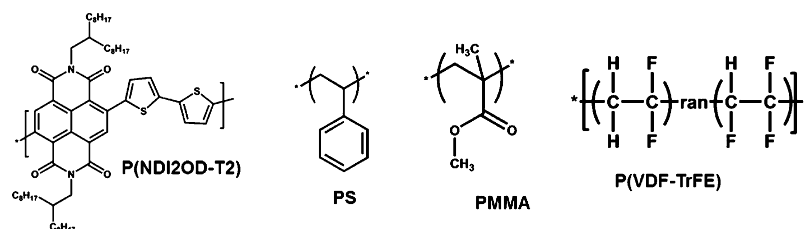

Figure 1. Molecular structures of P(NDI2OD-T2) as an ambipolar semiconductor, with PS, PMMA, and P(VDF-TrFE) as gate dielectrics.

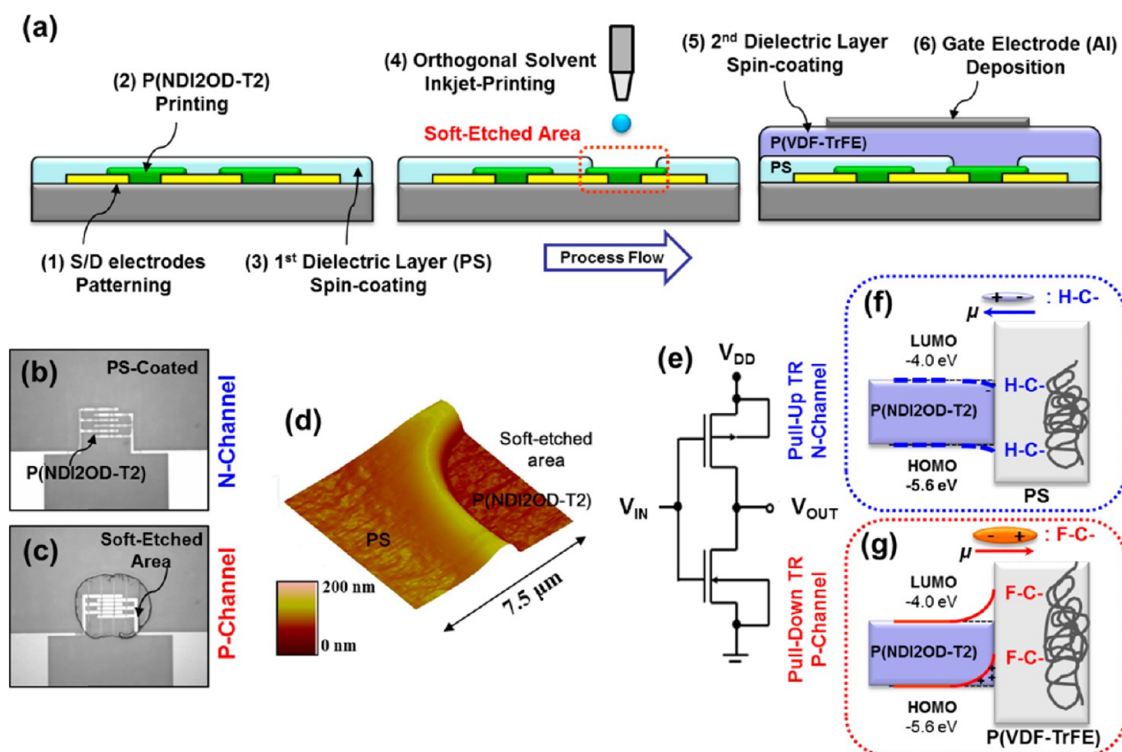

Figure 2. (a) Schematic diagram of the fabrication process for a complementary-like inverter device. Microscope images of (b) the PS-coated n-channel region and (c) PS soft-etched p-channel region for building a complementary-like inverter device based on the ambipolar P(NDI2OD-T2) semiconductor. (d) AFM image of soft-etched PS area on the P(NDI2OD-T2) layer shown in panel c. (e) Circuit configuration of the complementary-like inverter. Schematic illustration of the energy-band diagram in the gate-to-channel direction from the source/drain electrode for the (f) n-channel pull-up transistor and (g) p-channel pull-down transistor.

semiconductor energetic levels. In addition, the relatively high permittivity of P(VDF-TrFE) (ε ~10) effectively reduced the operating voltage of ambipolar ICs below 10 V. However, P(VDF-TrFE) or the blended gate dielectric with a high concentration of P(VDF-TrFE) reduced the electron μ_{FET} from 0.4 to 0.1 $cm^2 V^{-1} s^{-1}$ and increased V_{Th} of P(NDI2OD-T2) OFETs with PMMA or PS. Therefore, it was difficult to obtain both high electron and hole μ_{FET} at the same time using the high-k P(VDF-TrFE) dielectric to realize high-speed ambipolar complementary ICs.

A possible approach is the selective use of a patterned dielectric layer for p-channel and n-channel OFETs to extract the best performance of both OFETs in complementary ICs by using optimum dielectrics for hole and electron transporting. However, this approach requires additional processes such as photolithography for patterning of the gate dielectric layer.[15,16] Moreover, the patterning process of the gate dielectric layer by photoirradiation and a wet- or dry-etching process can incur serious damage to the underlying organic semiconductor in the top-gate, bottom-contact OFET geometry. Instead of the conventional photopatterning process, inkjet printing using the gate dielectric solution to form a thin dielectric film can be considered as another approach. There have been several reports on inkjet-printed dielectrics for OFETs.[17,18] However, it is difficult to obtain high-quality and robust dielectric thin films by inkjetting, and this approach faces several challenges including a nonuniform film surface by the strong coffee-ring effect, difficulty in the precise control of the dielectric film thickness by inkjet printing, and dissolution of the underlying semiconducting layer.[17] OFETs with rough dielectric layers exhibit poor device characteristics, with a large operating voltage, a relatively high gate-leakage current, and severe device-to-device performance deviation.[19,20] Therefore, sophisticated and mild patterning and processing of the gate dielectric layer is required to build highly densified complementary ICs using OFETs. However, representative graphic-art printing methods for uniform dielectric-layer coating, such as screen printing and bar coating, have relatively low resolutions of no more than a few hundred micrometers, which obviously limits the technique to low degrees of device integration per unit area in printed ICs.[21]

Herein, we report inkjet printing combined with soft-etching techniques for realizing high-performance printed and flexible organic ICs based on unipolar or ambipolar polymer semiconductors. The soft-etching method enables selective etching of gate dielectrics without any damage to the underlying conjugated polymer film and application of a more suitable dielectric layer for the p-channel and n-channel OFETs in complementary ICs. A hydrogenated polymer (PS or PMMA) is deposited by spin coating or other blanket-coating processes on a conjugated polymer film for overall coverage of the area, and the gate dielectric layer over the p-channel region is then selectively etched by inkjet printing the orthogonal solvent for the underlying polymer semiconductor. Finally, the fluorinated-P(VDF-TrFE) dielectric layer, which is a favorable dielectric for p-channel OFETs, is deposited by spin coating or another blanket-coating process on top of that layer. Through this method, p-channel (pull-up) and n-channel (pull-down) P(NDI2OD-T2) OFETs in ambipolar complementary ICs can each use their own favorable dielectric layer. We demonstrated the fabrication of high-speed, five-stage ambipolar ROs with a strong, n-type P(NDI2OD-T2) semiconductor. The best device exhibited a high oscillation frequency (f_{osc}) of ~16.7 kHz, which was highly improved from non-soft-etched ROs with a single P(VDF-TrFE) dielectric layer (~3 kHz).

EXPERIMENTAL SECTION

Materials and Device Fabrications. Inkjet-printed P(NDI2OD-T2) (Polyera Inc.) OFETs with PMMA (Aldrich), P(VDF-TrFE) (Solvay, 70:30 molar ratio random copolymer), and PS (Aldrich)/P(VDF-TrFE) as gate dielectrics were fabricated as previously reported.[13] For the fabrication of soft-etched OFETs, a pure solvent (nBA) was inkjet-printed on a channel region of a PS-coated device, and the P(VDF-TrFE) solution was spin-coated afterward.

Inverter and Ring Oscillator Fabrication. Au and Ni (12 and 3 nm thick, respectively) electrical-contact patterns were fabricated on the substrate using a conventional lift-off photolithography technique. After printing and thermal annealing of the semiconductor, the gate dielectric layers were spin-coated and thermally baked. To fabricate soft-etched inverters or ROs, after spin-coating of the first dielectric layer (PS) the nBA solvent was inkjet-printed on the p-channel mode transistors in circuits to etch the PS layer, and the second dielectric layer (P(VDF-TrFE)) was then spin-coated. 2-Butanone solvent was inkjet-printed on the device to make the via-hole structures of ROs. Finally, the devices were completed with Al gate electrodes (~500 nm thick) using a metal shadow mask.

Thin Film and Device Characterization. Atomic force microscopy (AFM) measurements were performed using a Digital Instruments Multimode atomic force microscope controlled by a Nanoscope IIIa scanning-probe microscope controller. Absorption spectra were measured using a Lambda 750 UV/vis spectrophotometer (PerkinElmer). The electrical characterization of the fabricated OFETs and the static characteristics of the complementary-like inverters were measured using a Keithley 4200-SCS in a nitrogen-filled glovebox under dark conditions. The output-voltage oscillation characteristics of the ROs were measured using a Keithley 4200-SCS with a built-in oscilloscope.

RESULTS AND DISCUSSION

Although P(NDI2OD-T2) was originally designed for n-channel OFETs, it consists of electron-rich bithiophene units and electron-deficient naphthalene-diimide units in a polymer backbone, as shown in Figure 1.[22] As a result, the electron donor−acceptor unit in the copolymer backbone exhibits intrinsically ambipolar charge transport with a high electron mobility of 0.3−0.8 $cm^2 V^{-1} s^{-1}$ and a low hole mobility of ~10^{-3} $cm^2 V^{-1} s^{-1}$ with commonly used polymer dielectrics (PMMA, PS, and CYTOP, an amorphous fluoropolymer). In our previous report, we demonstrated the systematic tuning of the ambipolar characteristics in P(NDI2OD-T2) OFETs using the fluorinated high-*k* polymer dielectric P(VDF-TrFE) or its blend with PMMA or PS. The P(NDI2OD-T2) OFETs with P(VDF-TrFE) exhibited a remarkably improved hole mobility of up to ~0.1 $cm^2 V^{-1} s^{-1}$ by sacrificing the electron mobility to a value below ~0.1 $cm^2 V^{-1} s^{-1}$.[13] To obtain the best device performance, PMMA, PS, or CYTOP was used for n-channel regions and P(VDF-TrFE) was used for p-channel regions in P(NDI2OD-T2) ambipolar OFETs and complementary ICs.

Table 1. Fundamental Parameters of Various Gate Dielectric Layers

dielectrics	thickness (nm)	ε_r	capacitance (nF cm^{-2})
PMMA	~125	3.5	~24.7
P(VDF-TrFE)	~230	10.4	~40.0
PS	~30	2.45	~72.3
PS/P(VDF-TrFE)	~30/~220	2.45/10.4	~23.8

In our current study, we developed an inkjet-printing method of orthogonal solvents for the selective etching of gate dielectric layers, and we applied the bilayered PS/P(VDF-TrFE) gate dielectric for n-channel OFETs and P(VDF-TrFE) for p-channel OFETs, as can be seen from the overall fabrication process in Figure 2a. It should be noted that proper selection of the orthogonal solvents is the most important consideration when constructing patterned gated dielectrics. We used *n*-butyl acetate (nBA) as an orthogonal solvent because it dissolves PS in the first dielectric layer without damaging the P(NDI2OD-T2) organic semiconductor layer. This procedure is referred to as the soft-etching process.

After sequential inkjet printing and thermal annealing of the semiconductor followed by the spin coating of the first gate dielectric layer (PS) over the entire area, pure nBA solvent was inkjet-printed onto the p-channel (pull-down) transistor region to remove selectively the PS dielectric. Figure 2b,c shows optical microscope images of the pristine and completely etched PS layer on the P(NDI2OD-T2) film by inkjet printing with nBA solvent. A P(VDF-TrFE) layer (as the favorable dielectric for the p-channel transistor) was spin-coated over the entire area, and, finally, the Al gate electrode was deposited by thermal evaporation with a metal shadow mask. Using this method, we could selectively apply two different dielectric layers, PS/P(VDF-TrFE) (for the n-channel) and P(VDF-TrFE) (for the p-channel), for the P(NDI2OD-T2) ambipolar complementary inverter (Figure 2e), which led to the effect of interfacial dipoles in the dielectric, enhancing the accumulation of negative- and positive-charge carriers at the P(NDI2OD-T2)−PS and P(NDI2OD-T2)−P(VDF-TrFE) interfaces, respectively, as shown Figure 2f,g.[13] The properties, including the thickness, dielectric constant, and capacitance values, of the gate dielectrics are summarized in Table 1.

The soft-etching process was obviously different from the conventional wet-etching process used in photolithography, which requires several procedures. After UV exposure using a photomask, the target material is removed by an etchant and the remnant is washed away from the substrate by a rinsing liquid.[23] Photoirradiation and a wet- or dry-etching process can cause serious damage to the underlying organic semiconductor during the conventional etching process. However, the soft-etching process is very simple. In both the via-hole and soft-

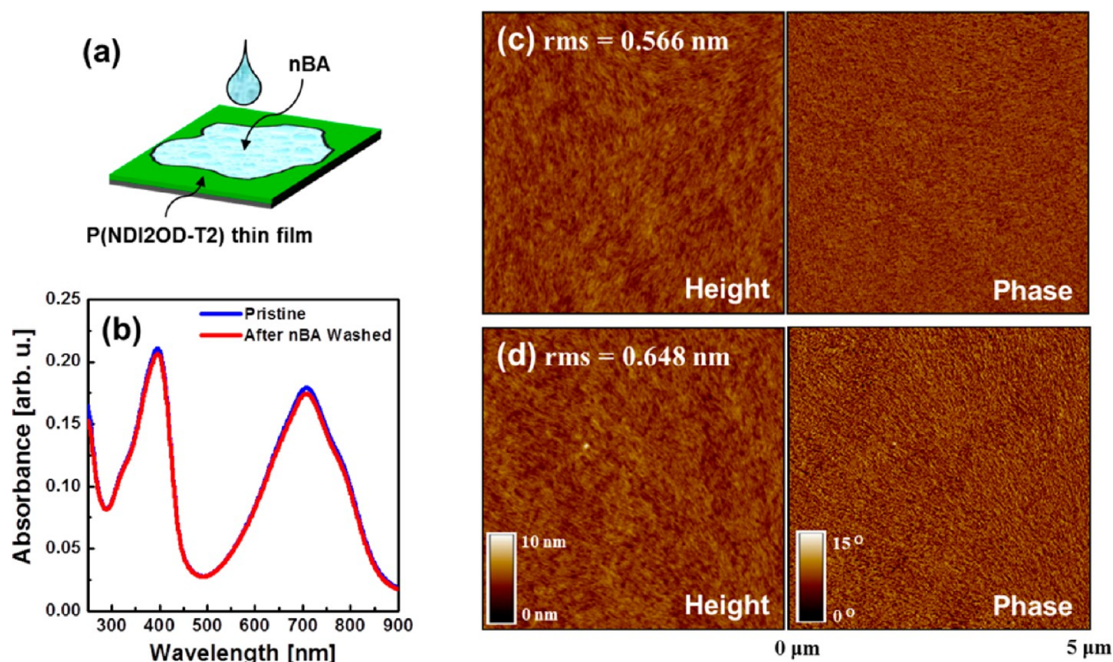

Figure 3. (a) Schematic diagram of the washing process of the P(NDI2OD-T2) thin film with nBA pure solvent. (b) UV/vis absorption spectra for pristine and nBA-washed P(NDI2OD-T2) films. AFM images (height and phase mode) of the spin-coated P(NDI2OD-T2) semiconductor films: (c) in a pristine state and (d) after release of the nBA pure-solvent droplets.

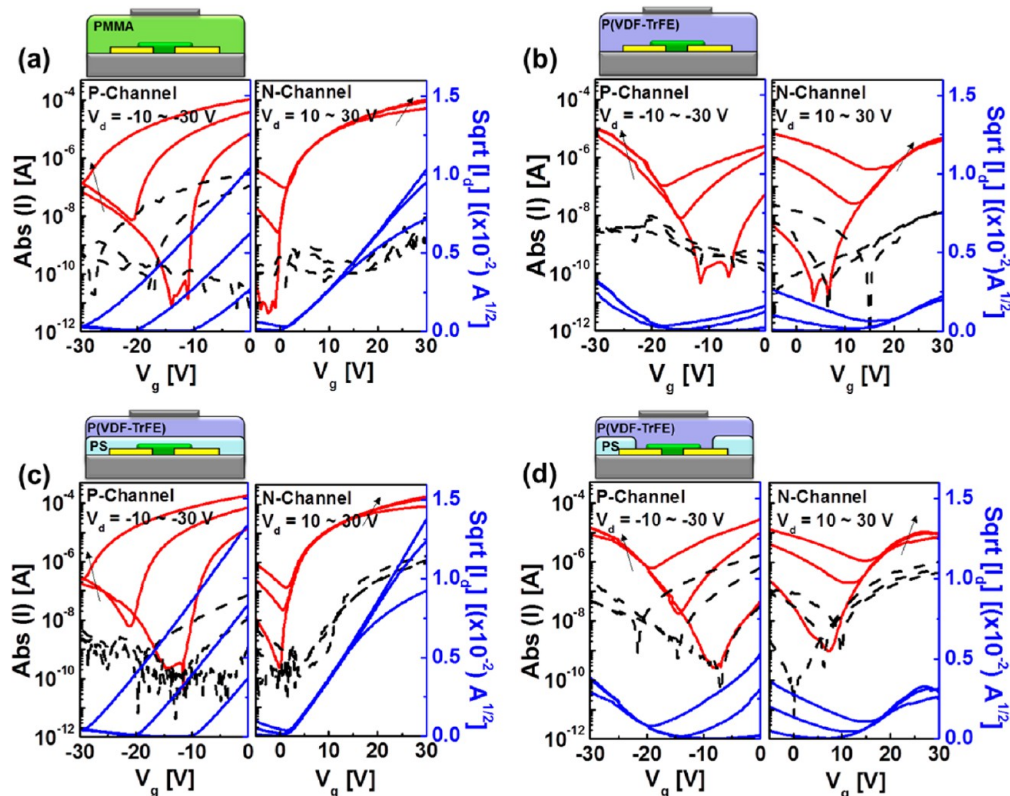

Figure 4. P-channel (at $V_d = -10$ to -30 V) and n-channel (at $V_d = 10$ to 30 V) transfer characteristics of the ambipolar P(NDI2OD-T2) OFETs using the (a) PMMA, (b) P(VDF-TrFE), (c) PS/P(VDF-TrFE) bilayer, and (d) PS soft-etched P(VDF-TrFE) gate dielectrics. The red solid, black dashed, and blue solid lines represent the drain current, I_d, gate current, I_g, and sqrt(I_d), respectively.

etching processes, the target material is dissolved as small volumes of the etching solvent are released in droplets followed by the flow of the dissolved solution from the center to the edge, with solidification occurring mostly in the edge region, which results in the formation of a crater-like hole because of the microfluid flow, as shown in the atomic force microscope (AFM) image in Figure 2d.[24−26] It should be noted that in the soft-etching process, the underlying semiconductor layer acts as

Table 2. Top-Gate/Bottom-Contact OFET Parameters for the Ambipolar P(NDI2OD-T2) Semiconductor with Various Gate Dielectric Layers[a]

dielectric layer	operation mode	mobility ($cm^2 V^{-1} s^{-1}$)	V_{Th} (V)	I_{on}/I_{off} at V_d = ± 10 V (±30 V)
PMMA	p-channel	~0.0022 ± 0.001	−20.1 ± 2.3	~10^4 (~10^1)
	n-channel	~0.25 ± 0.03	4.6 ± 1.5	~10^7 (~10^3)
P(VDF-TrFE)	p-channel	~0.093 ± 0.02	−19.3 ± 3.5	~10^5 (~10^2)
	n-channel	~0.050 ± 0.007	16.1 ± 2.1	~10^5 (~10^1)
PS/P(VDF-TrFE)	p-channel	~0.0064 ± 0.002	−20.9 ± 1.3	~10^4 (~10^1)
	n-channel	~0.39 ± 0.04	2.83 ± 1.1	~10^7 (~10^3)
P(VDF-TrFE), after soft-etched PS	p-channel	~0.10 ± 0.02	−18.8 ± 3.8	~10^5 (~10^2)
	n-channel	~0.047 ± 0.013	10.4 ± 0.3	~10^4 (~10^1)

[a]The values of μ_{FET} and V_{Th} were calculated at the saturation regime (V_d = ±30 V) using gradual channel-approximation equations (W/L = 1.0 mm/20 μm).

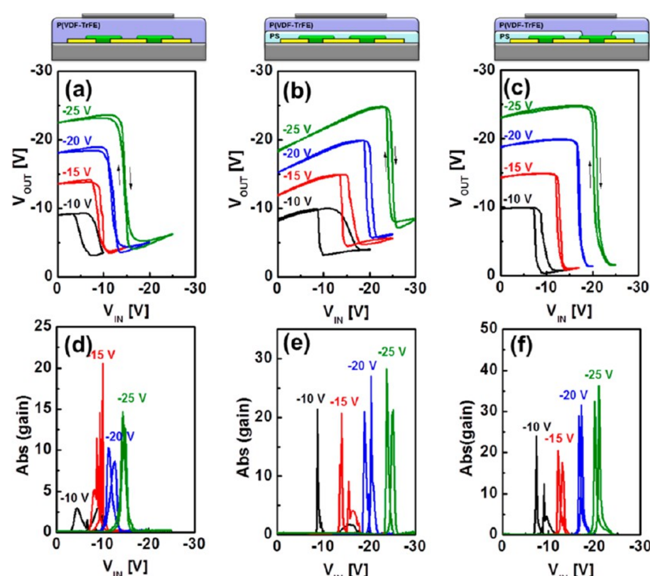

Figure 5. Complementary-like inverter characteristics. (a−c) Voltage transfer characteristics (VTCs) and (d−f) corresponding voltage gains of the complementary-like inverters based on ambipolar P(NDI2OD-T2) with various gate dielectrics: (a, d) P(VDF-TrFE), (b, e) PS/P(VDF-TrFE), and (c, f) soft-etched PS, P(VDF-TrFE) + PS/P(VDF-TrFE) (L = 10 μm, W_n/W_p = 1:1).

an etch-stopping layer. As shown in Figure 2d, a hill of approximately 40 nm in height and 2.5 μm in width was formed from the PS flow during the inkjet-etching process (for more detailed images of the hill, see Supporting Information Figure S1). An unintentionally large hill could have adverse effects on the uniformity of the dielectric layer in neighboring transistors in the TFT array and circuits. The size of the hill obtained by our etching process was negligible because the distance between the n- and p-channel transistors was about 500 μm in the device configuration (including the inverters and ROs). The height and width of the hills could be further reduced by decreasing the PS film thickness, and the size of etched area can be controlled by the volume of the etching solvent droplet. In addition, this process could be further optimized using a high-tech inkjet printer such as electrohydrodynamic (EHD) inkjet, which can be used to print high-resolution patterns.[27]

In top-gated OFETs, most of the charges flow through a few molecular layers at the semiconductor and dielectric interface, where the top surface of the semiconductor layer is located. This important top surface should be protected from any contamination or damage during the etching process, such as unwanted doping or swelling/dissolution of the semiconductor layer by the solvent, which would cause degradation of device performance. For this purpose, we chose nBA as the solvent because it is a good solvent to PS and it offers high orthogonality to the underlying P(NDI2OD-T2) polymer semiconductor as well as suitable surface tension and boiling point for the formation of stable solvent droplets during the inkjet-printing process. To verify the nBA etching solvent's effect on the semiconductor layer, the solvent resistance and surface morphology of the P(NDI2OD-T2) layer were characterized by UV/vis absorption spectra and AFM images after the pure nBA solvent was released onto the P(NDI2OD-T2) thin film, as illustrated in Figure 3a. The P(NDI2OD-T2) thin film showed no changes in the UV/vis absorption spectra after inkjet printing of nBA and natural drying (Figure 3b). In addition, Figure 3c,d shows the height- and phase-mode AFM images of the pristine P(NDI2OD-T2) surface as well as the surface after releasing the nBA solvent on the PS layer, respectively. Although the root-mean-square (rms) roughness of the P(NDI2OD-T2) surface increased slightly from 0.57 to 0.65 nm after washing with nBA, there was no significant morphological change, as shown in the AFM images. These results show that there was no noticeable change on the semiconductor active layer by the soft-etching process.

The gate dielectric effects of PMMA, P(VDF-TrFE), and PS/P(VDF-TrFE) on the transfer characteristics of P(NDI2OD-T2) OFETs are shown in Figure 4a−d. The measured fundamental parameters of P(NDI2OD-T2) OFETs, such as μ_{FET}, V_{Th}, and on/off-current ratio (I_{on}/I_{off}), are summarized in Table 2. On the basis of the gradual channel approximation, μ_{FET} was calculated for the saturation regime at a drain voltage (V_d) of 30 V (n-channel) or −30 V (p-channel). P(NDI2OD-T2) OFETs with the PMMA gate dielectric (Figure 4a) showed typical dominant characteristics of the n-channel, with high electron mobility of $\mu_{FET,e}$ = (0.25 ± 0.03) $cm^2 V^{-1} s^{-1}$ and very low hole mobility of $\mu_{FET,h}$ = (2.2 ± 1.0) × 10^{-3} $cm^2 V^{-1} s^{-1}$, which were consistent with previous reports.[13] However, the p-channel characteristics of P(NDI2OD-T2) OFETs showed remarkable enhancement through application of P(VDF-TrFE) as a dielectric layer, as shown in Figure 4b. P(NDI2OD-T2) OFETs with P(VDF-TrFE) exhibited high $\mu_{FET,h}$ of ~0.1 $cm^2 V^{-1} s^{-1}$, but at the same time $\mu_{FET,e}$ was reduced sharply to ~0.05 $cm^2 V^{-1} s^{-1}$. This was mostly attributed to the large dipole moment of the asymmetric fluorinated side chain in the P(VDF-TrFE) gate dielectric, which led to enhanced hole accumulation.[13] Interestingly, the hole accumulation by −C−F dipoles at the semiconductor−dielectric interface was completely suppressed by insertion of the thin PS layer between the

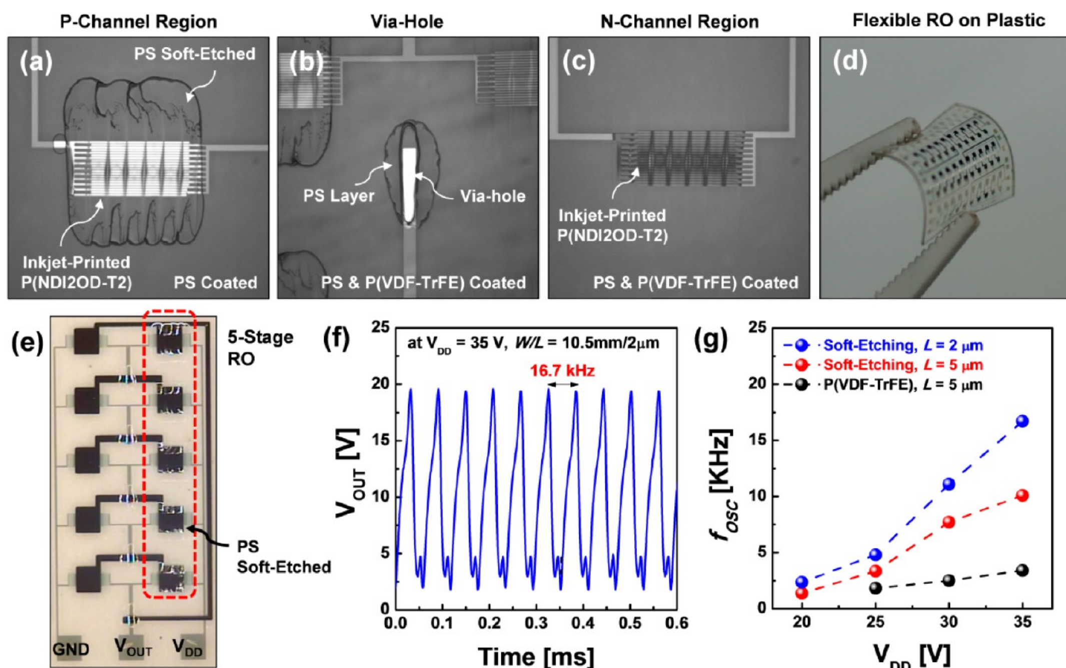

Figure 6. CCD camera images of the five-stage ambipolar ROs fabricated in the study: (a) PS soft-etched p-channel transistor region on inkjet-printed P(NDI2OD-T2) semiconductor layer, (b) via-hole area etched by 2-butanone solvent, and (c) PS/P(VDF-TrFE)-coated n-channel transistor region. (d) Digital camera image of the flexible printed RO fabricated on a PEN plastic substrate. (e) CCD camera images, (f) V_{OUT} oscillation characteristics at V_{DD} = 35 V, and (g) f_{osc} as a function of V_{DD} of the five-stage ROs using P(NDI2OD-T2) with soft-etched polymer gate dielectrics. The inverters have the same W_p/L_p and W_n/L_n ratios of 10.5 mm/(2 or 5 μm).

P(NDI2OD-T2) and P(VDF-TrFE) layers. The P(NDI2OD-T2) OFETs with bilayered PS/P(VDF-TrFE) gate dielectrics showed similar dominant characteristics of the n-channel with PMMA ($\mu_{FET,e}$ = ~(0.39 ± 0.04) $cm^2\ V^{-1}\ s^{-1}$ and $\mu_{FET,h}$ = ~(6.4 ± 0.002) × 10^{-3} $cm^2\ V^{-1}\ s^{-1}$), as shown in Figure 4c. Notably, the slightly better $\mu_{FET,e}$ of PS/P(VDF-TrFE) OFETs compared to that of PMMA devices was presumably attributed to a slightly larger charge-carrier concentration, which was due to a stronger electric field at the semiconductor active channel near the bilayered, low-*k*/high-*k* dielectrics.[28] Moreover, $\mu_{FET,e}$ in P(NDI2OD-T2) could be decreased with the high-*k* dielectric materials, leading to an increase in the activation energy of the charge carriers because of the strong interaction between the electrons in the channel and the ionic polarization cloud in the gate dielectric, the so-called "Fröhlich polaron" effect. The low-*k* PS interface was thus favorable to the charge transport of electrons in the P(NDI2OD-T2) thin film.[29−31]

After the soft-etching process with nBA solvent, the OFETs showed nearly the same properties as those of P(VDF-TrFE) devices ($\mu_{FET,h}$ = ~0.10 ± 0.02 $cm^2\ V^{-1}\ s^{-1}$ and $\mu_{FET,e}$ = ~0.047 ± 0.013 $cm^2\ V^{-1}\ s^{-1}$), as shown in Figure 4d, indicating that the PS layer was completely etched and that the P(NDI2OD-T2) active channel was not damaged electrically during the soft-etching process. Thus, by using the bilayered PS/P(VDF-TrFE) and single-layered P(VDF-TrFE) dielectrics for the respective n- and p-channel OFETs based on P(NDI2OD-T2), the maximum $\mu_{FET,e}$ and $\mu_{FET,h}$ as well as small $V_{Th,e}$ and $V_{Th,h}$ could be extracted for optimal OFET performances.

We constructed ambipolar P(NDI2OD-T2) complementary inverters with three different gate dielectrics: (1) PS/P(VDF-TrFE), (2) P(VDF-TrFE), and (3) soft-etched dielectric consisting of n-channel PS/P(VDF-TrFE) and p-channel P(VDF-TrFE). Figure 5 shows the voltage-transfer characteristics (VTCs) (a−c) and corresponding voltage gains (d− f) of these inverters at various values of supplied voltage (V_{DD}). At first, the ambipolar inverter with PS/P(VDF-TrFE) required a large inverting voltage (V_{inv}) far away from the ideal switching point at $^1/_2\ V_{DD}$ owing to the significantly different μ_{FET} and V_{Th} for the p- and n-channel operating regimes of the same ambipolar OFETs. Moreover, large V_{OUT} losses (6 to 7 V at V_{DD} = −20 V) at both the static on (at V_{IN} = 0 V) and off states (at V_{IN} = V_{DD}) of the inverter were driven because a large amount of the leakage current flowed through the pull-up (pull-down) transistor that was not completely turned off when the other pull-down (pull-up) transistor was turned on. In contrast, for an inverter with the P(VDF-TrFE) gate dielectric, V_{inv} showed the best value near $^1/_2\ V_{DD}$, which resulted from the relatively well balanced μ_{FET} and V_{Th} for the p- and n-channel operating regimes.

However, some amount of V_{OUT} loss at both the static on and off states was still observed. P(NDI2OD-T2) inverters with soft-etched dielectrics showed remarkably improved VTCs, with negligible V_{OUT} loss at V_{IN} = 0 V and less than 2 V at V_{IN} = −20 V (at V_{DD} = −20 V). This was mainly because the selectively patterned P(VDF-TrFE) (or PS/P(VDF-TrFE)) gate dielectrics induced p-channel (or n-channel)-dominant charge-transport properties while suppressing minority charge-carrier flows, which contributed to V_{OUT} of the ambipolar inverters. Through the dielectric optimization, the inverters with soft-etched gate dielectrics exhibited the highest gain of ~37 at V_{DD} = −25 V. It should be noted that V_{inv} of the soft-etched inverter was also shifted slightly from the $^1/_2\ V_{DD}$ value owing to the unbalanced μ_{FET} and V_{Th} of p- and n-channel operating regimes. With further optimized circuit geometry such as the transistor channel width/length ratio (*W*/*L*), V_{inv} could be controllable to $^1/_2\ V_{DD}$, thereby raising the signal-to-noise margin sufficiently to build digital logic gates.[32]

High-speed, five-stage ROs were built using the P(NDI2OD-T2) ambipolar semiconductor and gate dielectrics patterned with the soft-etching process. The via-hole connection was processed by another soft-etching process using 2-butanone as the solvent, which could dissolve both the PS and P(VDF-TrFE) layers (Figure 6a−c). The top-view image of the fabricated five-stage ROs and the corresponding V_{OUT} oscillation signal are shown in Figure 6e,f. The maximum f_{osc} of about 16.7 kHz was obtained at V_{DD} = 35 V, whose value was much higher than that of ROs with the single-layered P(VDF-TrFE) gate dielectric at the same V_{DD} and W/L (∼3.4 kHz). Moreover, soft-etched ROs were shown to initiate voltage oscillation under the relatively low bias condition of 20 V, whereas ROs with the P(VDF-TrFE) gate dielectric started to oscillate at more than 25 V. This remarkable enhancement of the RO speed was believed to have mostly resulted from increased values of $\mu_{FET,e}$ and $\mu_{FET,h}$ in individual optimized OFETs by using the patterned gate dielectrics obtained through soft etching. Furthermore, low-temperature and fast-etching processing using a multinozzle inkjet printer as well as web-based roll-to-roll processing enabled flexible and printed organic electronic devices on a plastic substrate. We demonstrated the fabrication of flexible or printed and air-stable ambipolar ICs on a poly(ethylene naphthalate) PEN (Tenjin DuPont Films) plastic substrate, as shown in Figure 6d. The electrical properties were almost similar to those of RO devices on a glass substrate, with a maximum f_{osc} of ∼15 kHz at V_{DD} = 35 V.

■ CONCLUSIONS

High-speed, flexible, ambipolar polymer ICs were developed by selective etching and application of the polymer gate dielectrics via an inkjet-printing-based etching process. The cost-effective etching process enabled selective deposition of the gate dielectrics, which were preferable for p-channel and n-channel operations in the same P(NDI2OD-T2) ambipolar semiconductor channel. The f_{osc} of ∼16.7 kHz was the highest value achieved in five-stage RO devices based on the ambipolar P(NDI2OD-T2) semiconductor, much higher than that of nonpatterned devices (∼3 kHz). In addition to these high-speed ICs, this printing-based etching method could also be utilized to develop a number of printed or flexible organic electronic and optoelectronic applications that require selective gate dielectrics or heterojunctions. For instance, monolithic printed, organic NAND flash memory requires different gate dielectric layers either for normal transistor operations or nonvolatile memory cells with polymeric gate electrets or metallic nanoparticles as nanofloating gates.[33]

■ ASSOCIATED CONTENT

Supporting Information

AFM image of soft-etched PS area on a P(NDI2OD-T2) layer, optical microscope image of a PS soft-etched transistor array on a glass substrate, and field-effect mobility for ambipolar P(NDI2OD-T2) semiconductors with various gate dielectric layers. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

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